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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,644	08/19/2003	Hideki Murayama		3750

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,644	MURAYAMA ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-29 and 31-46* is/are pending in the application.

4a) Of the above claim(s) *1-20* is/are withdrawn from consideration.

5)☒ Claim(s) *30* is/are allowed.

6)☒ Claim(s) *21-29 and 31-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/227,740.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed June 28, 2005. This amendment has been entered and carefully considered. Claims 21-46 remain pending in the application. Claims 1-20 have been cancelled. Claim 30 is allowed.

2. The rejection of claim 23 under 35 USC § 112 second paragraph is withdrawn due to the amendment filed June 28, 2005.

3. Applicant's arguments with respect to claims 21-29 and 31-46 have been fully considered but they are not deemed to be persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a)

> shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 21-29 and 31-46 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ninomiya (USPN: 5,764,968).

As per claim 21; Ninomiya teaches the invention as claimed including a computer system supporting a virtual memory system comprising processor 11 for generating an address of a virtual address system (e.g. see figure 1); a first main memory storing information which processor 11 accesses is taught as memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); a non-volatile storage is taught as EEPROM 34 storing configuration information regarding a second main memory to be hot plugged (e.g. see figure 2, column 7, lines 22 et seq.); the further limitation of a case for housing the processor, main memory and the non-volatile memory is known to be embedded in the system of Ninomiya as a standard features for covering and protecting computer elements which must be existed in any computer system including the computer system of Ninomiya; by this rationale, claim 1 is rejected;

As per claim 22, the further limitation of wherein the processor has an address translating unit translating virtual

addresses and physical addresses and outputs physical addresses representing a region of the first main memory (memory 13) is taught by Ninomiya to the extent that it is being claimed since when data being exchanged among memory 131 and modules on the docking station 30 (fig. 2); translation of addresses must occur for data matching; in addition, Ninomiya further discloses system memory 131 having different modules/banks (col. 4, lines 33 et seq.) being equivalent to the memory regions and wherein the processor (CPU 11) accesses memory modules by using address map in a register (control register 122) mapped in a configuration address space to output physical address for access system memory 131 of memory 13 (e.g. see column 4, lines 61 et seq.);

As per claim 23, Ninomiya discloses the control register 122 stores a part of a first/second page structure (configuration address space) for the DRAM modules of the system memory 131 wherein the CPU 11 access the control register 122 for addressing system memory 131 or expanded memory 132 of memory 13 (e.g. see figure 1, column 4, lines 33-67);

As per claim 24, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claim 25, Ninomiya discloses the connecting switch as being equivalent to the host-PCI bridge for connecting processor 11, system memory 131 and non-volatile storage (EEPROM 34) (e.g.

see figure 1);

As per claim 26; Ninomiya teaches the invention as claimed including a computer system supporting a virtual memory system comprising processor 11 for generating an address of a virtual address system (e.g. see figure 1); a first main memory which processor 11 accesses is taught as memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); a non-volatile storage is taught as EEPROM 34 storing configuration information regarding a second main memory to be hot plugged (e.g. see figure 2, column 7, lines 22 et seq.); the further limitation of a housing including the processor, main memory and the non-volatile memory is known to be embedded in the system of Ninomiya as a standard features for covering and protecting computer elements which must be existed in any computer system including the computer system of Ninomiya; by this rationale, claim 26 is rejected;

As per claim 27, Ninomiya clearly teaches that EEPROM 34 stores information necessary for hot insertion such as the attributes (address, DMA channels ... and the like (which including the memory SIZE as being claimed; e.g. see column 7, lines 24-25);

As per claims 28 and 29, Ninomiya clearly discloses the first main memory as system memory 131 having a hardware

configuration table/translation table 1312b for storing configuration/translation information (e.g. see figure 1) wherein the configuration/translation table further storing information associated with the hardware configuration of the system including the expanded memory (or second main memory) (e.g. see column 4, lines 29-31), the further limitation of wherein the processor has a unit translating logical-physical address and accesses the address translation for generating physical addresses is taught by Ninomiya to the extent that it is being claimed since when data being exchanged among memory 131 having different modules/banks (col. 4, lines 33 et seq.) and modules on the docking station 30 (fig. 2); translation of addresses must occur for data matching; by this rationale, the claims are rejected.

As per claim 31, Ninomiya discloses the connecting switch as being equivalent to the host-PCI bridge for connecting processor 11, system memory 131 and non-volatile storage (EEPROM 34) (e.g. see figure 1);

As per claim 32; Ninomiya teaches the invention as claimed including a computer system comprising a first main memory is taught as memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); processor 11 for processing information stored in memory

13 (e.g. see figure 1); a non-volatile storage is taught as EEPROM 34 storing configuration information regarding a second main memory to be hot plugged (e.g. see figure 2, column 7, lines 22 et seq.); the further limitation of a housing including the processor, main memory and the non-volatile memory is known to be embedded in the system of Ninomiya as a standard features for covering and protecting computer elements which must be existed in any computer system including the computer system of Ninomiya; by this rationale, claim 32 is rejected;

As per claims 33 and 34, Ninomiya discloses the non-volatile storage stores memory size information of the first or second main memory as being equivalent EEPROM 34 stores information necessary for hot insertion such as the attributes (address, DMA channels ... and the like (which including ***the memory SIZEs*** *including the first and second main memory as being claimed*; e.g. see column 7, lines 24-25);

As per claim 35, Ninomiya clearly discloses the first main memory as system memory 131 having logical-physical address translation pair as a hardware configuration table/translation table 1312b and 1312a for storing configuration or translation information (e.g. see figure 1) wherein the configuration/ translation table pairs 1312a and 1312b further storing information associated with the hardware configuration of the system including the expanded memory (or second main memory)

(e.g. see column 4, lines 29-31);

As per claim 36, the further limitation of wherein the processor has a unit translating logical-physical address which uses the logical-physical address translation pair (hardware configuration table/translation table 1312b and 1312a) is taught by Ninomiya to the extent that it is being claimed since when CPU 11 requests data from storage memory 13 which utilized table 1312a and 1312b and data from docking station 30, data must be exchanged among memory 131 having different modules/banks (col. 4, lines 33 et seq.) and modules on the docking station 30 (fig. 2); translation of addresses must occur for data matching; by this rationale, the claims are rejected.

As per claims 37 and 38, Ninomiya discloses the untranslatable/translatable region of the first main memory (system memory 131) as being corresponded to the used/unused RAS lines for unused/used banks (e.g. see column 9, lines 29 bridging column 10, line 30);

As per claim 39, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claim 40, Ninomiya discloses the connecting switch as being equivalent to the host-PCI bridge for connecting processor 11, system memory 131 and non-volatile storage (EEPROM 34) (e.g. see figure 1);

As per claim 41; Ninomiya teaches the invention as claimed including a computer system for allowing a main memory to be hot-added while the computer is powered on comprising a first main memory is taught as memory 13 comprises system memory 131 mounted in advance on the system board, and an expanded memory 132 mounted by the user as needed (e.g. see figure 1, column 4, lines 22 et seq.); processor 11 for accessing system memory 131 thru a host-PCI bridge 12 (e.g. see figure 1); a non-volatile storage is taught as EEPROM 34 storing configuration information regarding a main memory to be hot plugged (e.g. see figure 2, column 7, lines 22 et seq.); the further limitation of a body housing the processor, the first main memory and the non-volatile memory is known to be embedded in the system of Ninomiya as a standard features for covering and protecting computer elements which must be existed in any computer system including the computer system of Ninomiya; by this rationale, claim 41 is rejected;

As per claim 42, Ninomiya clearly discloses the nonvolatile memory 34 is an EEPROM (e.g. see figure 2; column 7, lines 23 et seq.);

As per claim 43, Ninomiya discloses the connecting switch as being equivalent to the host-PCI bridge for connecting processor 11, system memory 131 and non-volatile storage (EEPROM 34) (e.g. see figure 1);

As per claim 44, Ninomiya clearly discloses the first main

memory as system memory 131 having logical-physical address translation pair as a hardware configuration table/translation table 1312b and 1312a for storing configuration or translation information (e.g. see figure 1) wherein the configuration/ translation table pairs 1312a and 1312b further storing information associated with the hardware configuration of the system including the expanded memory (or second main memory) (e.g. see column 4, lines 29-31);

As per claim 45 and 46, Ninomiya discloses the untranslatable/translatable region of the first main memory (system memory 131) as being corresponded to the unused/used RAS lines for unused/used banks (e.g. see column 9, lines 29 bridging column 10, line 30); wherein it's inherently known that the unused banks are being utilized to store processing data including the translating address table as being claimed since only the unused RAS line are being supplied and enabled by the memory clock (e.g. see column 9, lines 60 et seq.);

6. Claim 30 is now allowed. The prior arts of record do not teach nor disclose the first main memory (system memory 131) for storing address translation in a top priority region of interrupt handling and assigns the first region in the top priority region.

7. As per remark, Applicant's counsel asserts that (a) the

reference does not specifically disclose or suggest main memory or second main memory to be hot-added, hot plugged or hot inserted, as required by each of the independent claims; rather, the office action cites another memory disclosed in Ninomiya, that would be connected through card dock 40 as "part of main memory" that is able to be hot plugged, wherein the memory of a PC card, etc. and the main memory or second memory claimed by Applicants are not equivalent (amendment, page 14, second paragraph bridging page 15, first paragraph); and (b) the EEPROM 34 does not store memory size information of the (second) main memory to be hot plugged (amendment's page 15, second paragraph).

With respect to (a); first of all, it should be noted that Applicant never detailed nor disclosed the relationship between first main memory and second main memory; by simply recite "second main memory" does not mean that the second memory is part of the first main memory as being contended by Applicant's counsel. With that, the second main memory as being claimed by Applicant is well equivalent to either expanded memory 132 (e.g. see column 4, lines 34 et seq.) or PC/expansion memory card (e.g. see column 7, lines 25 et seq.). With respect to (b) Ninomiya clearly discloses the EEPROM 43 for storing hot-insertion information, e.g. information necessary for plug and play, this information is clearly and known to be available to the system prior to hot-inserted, for example, attributes or information of

the PC cards mounted in the expansion slots mentioned and detailed above (e.g. column 7, lines 46 et seq.).

8. Applicant's arguments filed June 28, 2004 have been fully considered but they are not deemed to be persuasive.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be

obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/September 16, 2005

Tuan V. Thai
PRIMARY EXAMINER
Group 2100